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	EXAMINER
26384 7590 11/09/2004	BANANKHAH, MAJID A

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DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _13 April 2001_.

2a) ☐ This action is **FINAL**.   2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
  closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-59_ is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-59_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a) ☐ All   b) ☐ Some * c) ☐ None of:

       1. ☐ Certified copies of the priority documents have been received.

       2. ☐ Certified copies of the priority documents have been received in Application No. _____.

       3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage
  application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
  Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   This office action is in response to application filed on January 12 2001. Applicants

electing the claims of group (I) without traverse are acknowledged. Claims 1-59, and the newly

added claims 24-29 are presented for examination.

Claim Rejections - 35 USC § 112

2.   Claims 26-28, 32, and 46-52, and 58 are rejected under 35 U.S.C. 112, second paragraph,

as being indefinite for failing to particularly point out and distinctly claim the subject matter

which applicant regards as the invention.

Per claims 26, the claim recite "said sending" and there is not sufficient antecedent basis

for this in the claims. Claims 27-28, and 32 are rejected for similar reasons.

In claim 37, the statement "prior to executing the critical section instruction" does not

have sufficient antecedent basis. In the first step, the critical section is just detected and not

executed. Additionally, if the critical section is associated with the network data running on the

first processing element, the relationship between the first processing element and the second

processing element is unclear. In the thirst step the execution of the critical section instruction is

suspended. There is no execution happening in the first two steps. Relationship between the three

steps is missing. It is unclear which processing element is executing the instruction. Claims 38-

45 are rejected for the rejection of their parent claim.

The claim is indefinite because in the first step the processing of a task is suspended in

response to detection of a critical section of the task. Later the processing of the task is resumed

in response to a critical section end signal received from a second processing element. While the

task is running on the first processing element, and there is no connection between the first

processing and the second processing elements, why the critical end signal should be received

from the second processing element. These steps are disjoint and are not connected. It is unclear

whether the two critical sections (critical section of the task, and critical section end signal) are

the same or different. Claims 47-52 are rejected for the rejection of their parent claim.

Claim 58 is rejected for the same reasons stated in the rejection of claim 37.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.   Claims are rejected under 35 U.S.C. 103(a) as being unpatentable over Iwasaki et al (US

Pat. No. 5,274,809, hereinafter Iwasaki).

Per claims 1, 12, and 59 an apparatus for processing information wherein processing

operations include a plurality of tasks, at least one of the plurality of tasks having a critical

section, the apparatus comprising (*the system of Iwasaki, col. 1, lns. 48-57, and col. 3, lins. 35-*

44):

a first processing element, said first processing element including:

a critical section end detector, and a critical section end signal generator coupled to said

critical section end detector (*col. 3, lns. 35-44, post issue task, and is released, whena*

shared resource is released upon completion of the use and a third task is allowed to lock the resource, the indication of the completion is indication of a "end of use of shared resource" [end detector], and when another task is allowed to use the shared resource a signal is forwarded to the other task that the resource is available [end signal generated]); and

a second processing element, said second processing element coupled to said first processing element and including *(the system of Iwasaki is a multiprocessor, and see abstract, where the shared resource is given to another processor),*

a critical section detector *(see col. 2, lns. 62-68, post issue task and post receive task, when the shared resource is in use any task trying to acquire the shared resource will detect that the resource is locked [shared resource locked section detector]*) and

a critical section processing controller, said critical section processing controller responsive to a critical section end signal received from said first processing element *(col. 10, lns. 26-40, wait post mechanism of Iwasaki).* The system of Iwasaki while teaches the use of shared resource among plurality of tasks, fails to teach of critical section, which by definition in the specification on page 19 "is an instruction or series of instructions that utilize a shared resource". However, it is well known that a task is composed of subtask, which is a sequence of instructions that can be executed by a computer. Therefore, the mechanism of Iwasaki is applicable with subtasks and/or sequence of instruction when using a shared resource. Therefore, it would have been obvious for one ordinary skill in the art at the time the invention was made to us the task execution control method of Iwasaki for a sequence of instruction using sharing resources.

Regarding the limitation of a ring of processing elements in claim 59, the system of Iwasaki does not preclude a ring of processing elements and the first processing element being upstream with respect to the second processing element, and this modification does not decrease the functionality of the system. Therefore, it would have been obvious to use the processing elements in a ring or loop arrangement for the reason to use the resource in series and reduce overhead due to simplicity of the arrangement.

Per claims 2, and 18, the apparatus of claim 1, said second processing element further including a counter, said critical section processing controller incrementing said counter in response to a critical section end signal (col. 10, lns. 41-45).

Per claims 3, and 19 the apparatus of claim 1, said second processing element further including a counter, said critical section processing controller decrementing said counter based on the detection of a critical section (col. 10, lns. 41-45).

Per claims 4, 14, and 20 the apparatus of claim 1, said second processing element further including a counter, said critical section processing controller suspending issuing instructions when said counter includes a value less than a threshold. While the system of Iwasaki teaches of suspending execution of a task he fails to teach using counter threshold for suspending the execution of a critical section. However, it is well known in the art to use a counter for issuing instruction for the purpose of detecting an event. Therefore, it would have been obvious for one

ordinary skill in the art at the time the invention was made to use a counter threshold for

triggering the issuance of instruction.

Per claim 5, the apparatus of claim 1, wherein said first processing element sends a

critical section end signal to said second processing element in response to processing an

instruction identifying an end of a critical section (*col. 3, lns. 35-44, post issue task, and is

released*).

Per claims 6-7, and 15 the apparatus of claim 1, wherein said second processing element

suspends processing a task in response to said critical section detector detecting a critical section

(col. 5, lns. 46-62).

Per claim 8, the apparatus of claim 7, wherein a critical section instruction identifies a

beginning of a critical section in the task at said second processing element (col. 1, lns. 58 to col.

2, lns., 2, using instruction in lock management).

Per claim 9, the apparatus of claim 7, wherein the critical section includes an instruction

that accesses a shared variable (Iwasaki, Abs.).

Per claim 10, the apparatus of claim 7, wherein the critical section includes an instruction

that accesses a shared peripheral. It is well known in that shared resource could be

software and/or hardware peripherals. It is obvious that the system of Iwasaki works with

software as well as hardware resource because he does not exclude the hardware

peripherals.

Per claims 11, and 13 the apparatus of claim 1, wherein said critical section end signal

generator

generates a critical section end signal in response to said critical section end detector (*col. 3, lns.*

35-44, post issue task, and is released).

Per claims 16, 17, and 53, the claims are rejected for the same reasons as stated in the

rejection of claims 1, and 12, however, the system of Iwasaki does not preclude a ring of

processing elements and the first processing element being upstream with respect to the second

processing element, and this modification does not decrease the functionality of the system.

Therefore, it would have been obvious to use the processing elements in a ring or loop

arrangement for the reason to use the resource in series and reduce overhead due to simplicity of

the arrangement.

Per claims 21, 37, and 58 a method for processing tasks on multiple processing elements

(*the system of Iwasaki, col. 1, lns. 48-57, and col. 3, lins. 35-44*), comprising:

processing a task on a first processing element (post issue task, col. 5, 1-25, and lns. 46-61);

inhibiting processing of a task on a second processing element based on processing a

critical section instruction at the second processing element (col. 5, lns. 46-61);

receiving a critical section end signal at the second processing element, the critical

section end signal indicating completion of processing of a critical section of a task at another

processing element (col. 5, lns. 1-25); and resuming processing the task at the second

processing element based on the critical section end signal (col.2, lns. 15-27, suspend/resume

mechanism, and col. 12, lins. 15-31). The system of Iwasaki while teaches the use of shared

resource among plurality of tasks, fails to teach of critical section. However, it is well known that

a task is a composition of subtasks and instructions. Therefore, the mechanism of Iwasaki is

applicable with subtasks and/or series of instruction using a shared resource. Therefore, it would

have been obvious for one ordinary skill in the art at the time the invention was made to us the

task execution control method of Iwasaki for a series of instruction using sharing resources.

Regarding the limitation of suspending execution of the critical section when said end

critical section signal counter is not above a threshold value in claim 37, it is well known in that

art to use counter and an upper limit (such as above a threshold value determined by the counter)

on the number of use of a task for accessing a shared resource for the reason to stop

monopolizing the resource by one task running on a processor. Therefore, it would have been

obvious for one ordinary skill in the art at the time the invention was made to use a upper limit

such as a threshold on the number of access time of one processor over a shared resource in order

to increase efficiency and let every task use the shared resource.

Per claim 22, the method of claim 21, wherein said inhibiting occurs substantially at a

beginning of a critical section of the task at the second processing element (*col. 9, lns. 33-36, as*

soon as the shared resource is locked any other task is inhibited from acquiring that resource).

Per claim 23, the method of claim 21, wherein said resuming occurs substantially at an

end of a critical section of the task at the first processing element. In the system of Iwasaki, the

resuming is at the end of the use of the shared resource by a task at another processing element
when a suspension period is over (col. 9, lns. 33-36).

Per claims 24-25, and 29-30, it is well know in the art at the time the invention was made to
associate the processors in a multiprocessing environment to network connection for the reason
that it will speed up the network switching process and change the functionality of the network
switching without changing the hardware. Therefore it would have been obvious for a person
ordinary skill in the art at the time the invention was made to implement the task execution
control method for the multiprocessing system of Iwasaki for the purpose of saving time and
increasing efficiency.

Per claim 26-28, and 32, the claims are rejected under 35 USC 112 second paragraph for the lack
of antecedent basis, and for the reasons explained in section 2 (*supra*), the Examiner cannot
apply art to these claims. It is unclear what "sending" the claim is referring to.

Per claim 31, the method of claim 21, wherein the task at the first processing element and
the task at the second processing element are associated with ordered data elements. The system
of Iwasaki, the tasks at the processing elements are associated with any data elements including
ordered data element, and this does not change the steps of its method.

Per claim 33, the method of claim 21, wherein said inhibiting occurs in response to
processing a critical section instruction. The locking mechanism that prevents another task from

accessing the resource is occurring when a first task on another processing element is using that resource. Therefore, inhibiting is in fact in response to the use of the shared resource by another processor task.

Per claim 34, the method of claim 33, wherein the critical section instruction identifies a beginning of a critical section in the task at the second processing element (see Iwasaki, col. 14, lines 3-18).

Per claim 35, he method of claim 33, wherein the critical section instruction is an instruction accessing a shared variable (reading the lock word, col. 14, lines 3-18)

Per claim 36, the method of claim 33, wherein the critical section instruction is an instruction accessing a shared peripheral. It is well known in the art that resource could be software as well as hardware, and the method of Iwasaki, is applicable to both resources for the reason that the method of Iwasaki need not be altered when the resources are hardware such as peripherals.

Per claim 38, please see the rejection of claim 22,

Per claim 39, please see the rejection of claim 23.

Per claim 40-41, please the rejection of claim 37 above regarding the use of the counter and implementing upper limit counter on the number of use of the shared resource.

Per claims 42-43, the method of claim 37, wherein said suspending occurs in response to processing a critical section instruction, and wherein the critical section instruction identifies a beginning of a critical section in the task at the first processing element (Iwasaki, col. 14, lines 3-18.

Per claim 44, please see the rejection of claim 35.

Per claim 45, please see the rejection of claim 36.

Per claim 46, please see the rejection of claim 21 regarding suspending and resuming of a processing of tasks. See also Iwasaki's background in col. 3, line 62 to col. 4, line 2.

Per claim 47, the method of claim 46, wherein the first processing element and the second processing element are coupled within a ring of processing element. The method of Iwasaki is applicable to a ring of processing element as well, for the reason that a ring of processing element does not alter the steps of the method.

Per claim 48-49, please see the rejection of claims 40-41.

Per claim 50, please see the rejection of claim 39.

Per claim 51, please see the rejection of claims 37, 40-41 regarding the counter and upper limit value on the number of times a shared resource is accesses.

Per claim 52, please see the rejection of claim 47.

Per claim 54, the apparatus of claim 53, wherein said first processing element is adjacent

to said second processing element in said ring of processing elements.

Per claim 55, please see the rejection of claim 38.

Per claim 56, please see the rejection of claim 35.

Per claim 57, please see the rejection of claim 36.

Conclusion

5.   The prior art made of record and not relied upon is considered pertinent to applicant's

disclosure

6.   Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Majid A. Banankhah** whose telephone number is (571) **272-3770**. The examiner can normally be reached on Monday – Thursday, 8:00 AM – 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756.

Information regarding the status of an application may be obtained from the patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll free).

Maid Banankhah
5/17/04

MAJID BANANKHAH
PRIMARY EXAMINER